IN THE CLAIMS:

Claim 6. (currently amended) A method of fabricating a semiconductor device having a semiconductor resistance element, comprising:

a step of doping an n-type impurity in a selected region in the surface of a semi-insulating compound semiconductor substrate via a first mask layer formed on the surface of the compound semiconductor substrate, to form an n-type impurity doped region;

a step of doping, after or before said step of forming the n-type impurity doped region, a p-type impurity in the surface of said compound semiconductor substrate via a second mask layer formed on the surface of said compound semiconductor substrate, to form a p-type impurity doped region;

a step of heat-treating the compound semiconductor substrate, to activate the impurities in the n-type impurity doped region and the p-type impurity doped region, thereby forming an n-type semiconductor resistance region, and also forming a p-type buried region between the n-type semiconductor resistance region and a substrate region of the semiconductor substrate in such a manner as to bring the p-type buried region into contact with the n-type semiconductor resistance region, wherein an impurity concentration of the p-type buried region is lower than that of the n-type semiconductor resistance region and higher than that of the compound semiconductor substrate in order to set a complete depleted state; and

a step of forming ohmic electrodes in the semiconductor resistance region.

Claim 7. (original) A method of fabricating a semiconductor device having a semiconductor resistance element according to claim 6, wherein the n-type impurity doped region and the p-type impurity doped region are formed in self-alignment by commonly using one mask layer as the first and second mask layers.